Claims

[c1] What is claimed is:

1.A method for monitoring a tunnel oxide layer, the method comprising:

(a)providing a semiconductor substrate, forming at least one memory cell on a surface of the semiconductor substrate, the memory cell comprising a first gate, a second gate, and the tunnel oxide layer from top to bottom in a stack;

(b)electrically connecting the first gate and the second gate;

(c)applying a first gate voltage to the first gate, the first gate voltage being a swing time-dependent DC ramping voltage;

(d)measuring a first gate leakage current of the memory cell to calculate a first constant from an equation;

(e)applying a second gate voltage to the first gate, the second gate voltage being a swing time-dependent DC ramping voltage;

(f)measuring a second gate leakage current of the memory cell to calculate a second constant from the equation;

(g)calculating a first ratio of the second constant to the first constant; and

(h)performing a comparing step to compare the value of the first ratio with a predetermined value.

[c2] 2.The method of claim 1 wherein the semiconductor substrate is a silicon substrate of a semiconductor wafer and the memory cell is formed in the testing area of the semiconductor wafer.

[c3] 3.The method of claim 1 wherein the memory cell is a flash memory cell, the first gate and the second gate are a controlling gate and a floating gate of the flash memory cell respectively.

[c4] 4.The method of claim 1 wherein the memory cell is a non-volatile memory cell, the first gate and the second gate are a controlling gate and a floating gate of the non-volatile memory cell respectively.

[c5] 5.The method of claim 1 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

[c6] 6.The method of claim 1 wherein the equation is the Fowler-Nordehim tunneling mechanism equation.

[c7] 7.The method of claim 1 wherein the predetermined value is 10.

[c8] 8.The method of claim 1 wherein each constant is a β value corresponding to each gate voltage respectively.

[c9] 9.The method of claim 8 wherein the first constant is a β 1 value corresponding to the first gate voltage, the β 1 value is equal to [{ Δ ln[|the first gate leakage current|/(|the first gate voltage|-|a flatband voltage(V_{fb})|)^2]} ÷ { Δ [1 ÷ first gate voltage|-|the flatband voltage|)]}] .

[c10] 10.The method of claim 8 wherein the second constant is a β 2 value corresponding to the second gate voltage, the β 2 value is equal to [{ Δ ln[|the second gate leakage current|/ |the second gate voltage|-|the flatband voltage(V_{fb})|)^2]} ÷ { Δ [1 ÷ (|the second gate voltage|-|the flatband voltage|)]}].

[c11] 11.The method of claim 8 further comprises the following steps when the value of the first ratio is not greater than the predetermined value:
applying a third gate voltage to the first gate, the third gate voltage is a swing time-dependent DC ramping voltage;
measuring a third gate leakage current of the memory cell to calculate a third constant from the equation;
calculating a second ratio of the third constant to the second constant; and
performing the comparing step to compare the value of the second ratio with the predetermined value.

[c12] 12.The method of claim 11 wherein the steps (c) to (h) are repeated when the value of the second ratio is not greater than the predetermined value.

[c13] 13.The method of claim 11 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

[c14] 14.The method of claim 11 wherein the third constant is a β 3 value

corresponding to the third gate voltage, the β 3 value is equal to [{ Δ ln[|the third gate leakage current|/ (|the third gate voltage|-|a flatband voltage(V_{fb})|) ^{2}]} ÷ { Δ [1 ÷ (|the third gate voltage|-|the flatband voltage|)]}] .

[c15] 15.The method of claim 14 further comprises a step for plotting a β -V_g curve of each β value respectively corresponding to the first gate voltage, the second gate voltage and the third gate voltage versus the first gate voltage, the second gate voltage and the third gate voltage, a reference β -V_g curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the β -V_g curve to monitor the quality of the tunnel oxide layer.

[c16] 16.The method of claim 15 wherein the β -V_g curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

[c17] 17.The method of claim 16 wherein the β value within the first region is zero to represent each gate leakage current flowing through the first gate and the second gate in the memory cell being less than a predetermined current value, the absolute value of the β value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each gate leakage current of the memory cell, the β value within the third region crosses the reference β -V_g curve to represent a plurality of carriers being trapped by the tunnel oxide layer.

[c18] 18.The method of claim 17 wherein the predetermined current value is $1.0x10^{-11}$ A.

[c19] 19.The method of claim 8 further comprises a step for plotting a β -V_g curve of each β value versus each gate voltage, a reference β -V_g curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the β -V_g curve to monitor the quality of the tunnel oxide layer.

[c20] 20.The method of claim 1 wherein the method is applied to a wafer acceptance testing (WAT) equipment to fast monitor the stress-induced degradation of the tunnel oxide layer in the memory cell.

[c21] 21.A method for fast monitoring the stress-induced degradation of an oxide

layer by a wafer acceptance testing (WAT) equipment, the method comprising:

(a) providing a semiconductor substrate, a surface of the semiconductor substrate comprising the oxide layer and a first gate disposed on the oxide layer;

(b) applying a first gate voltage to the first gate, the first gate voltage being a swing time-dependent DC ramping voltage;

(c) measuring a first gate leakage current flowing through the first gate to calculate a first proportional value from the first gate voltage, the first gate leakage current, and an equation, the first proportional value corresponding to the first gate voltage;

(d) applying a second gate voltage to the first gate, the second gate voltage being a swing time-dependent DC ramping voltage;

(e) measuring a second gate leakage current flowing through the first gate to calculate a second proportional value from the second gate voltage, the second gate leakage current, and the equation, the second proportional value corresponding to the second gate voltage; and

(f)calculating a first ratio of the second proportional value to the first proportional value.

[c22] 22.The method of claim 21 wherein the semiconductor substrate is a silicon substrate of a semiconductor wafer and the first gate is formed in the testing area of the semiconductor wafer.

[c23] 23.The method of claim 21 wherein a second gate is formed between the first gate and the oxide layer.

[c24] 24.The method of claim 23 further comprises an electrically connecting step performed before applying the first gate voltage to the first gate to electrically connect the first gate and the second gate.

[c25] 25.The method of claim 24 wherein the memory cell is a flash memory cell, the first gate and the second gate are a controlling gate and a floating gate of the flash memory cell respectively.

[c26] 26.The method of claim 24 wherein the first gate is a controlling gate of the

flash memory cell, the second gate is a floating gate of the flash memory cell, the oxide layer is a tunnel oxide layer of the flash memory cell.

[c27] 27.The method of claim 21 wherein the first gate is a gate of a metal-oxide-semiconductor (MOS) transistor, the oxide layer is a gate oxide layer of the MOS transistor.

[c28] 28.The method of claim 21 further comprises a comparing step to compare the value of the first ratio with a predetermined value.

[c29] 29.The method of claim 28 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

[c30] 30.The method of claim 28 wherein the predetermined value is 10.

[c31] 31.The method of claim 21 wherein the equation is the Fowler-Nordehim tunneling mechanism equation.

[c32] 32.The method of claim 21 wherein each proportional value is a β value corresponding to each gate voltage respectively.

[c33] 33.The method of claim 32 wherein the first proportional value is a β 1 value corresponding to the first gate voltage, the β 1 value is equal to [{ Δ ln[|the first gate leakage current|/(|the first gate voltage|-|a flat band voltage(V_{fb})|)^2]} ÷ { Δ [1 ÷ (|the first gate voltage|-|the flat band voltage|)]}].

[c34] 34.The method of claim 32 wherein the second proportional value is a β 2 value corresponding to the second gate voltage, the β 2 value is equal to [{ Δ ln[|the second gate leakage current|/ (|the second gate voltage|-|the flatband voltage (V_{fb})|)^2]} ÷ { Δ [1 ÷ (|the second gate voltage|-|the flatband voltage|)]} .

[c35] 35.The method of claim 32 further comprises the following steps when the value of the first ratio is not greater than the predetermined value:
applying a third gate voltage to the first gate, the third gate voltage is a swing time-dependent DC ramping voltage;
measuring a third gate leakage current flowing through the first gate;

calculating a third proportional value from the third gate voltage, the third gate leakage current, and the equation, the third proportional value corresponding to the third gate voltage;

calculating a second ratio of the third proportional value to the second proportional value; and

performing the comparing step to compare the value of the second ratio with the predetermined value.

[c36] 36.The method of claim 35 wherein the steps (b) to (f) are repeated when the value of the second ratio is not greater than the predetermined value.

[c37] 37.The method of claim 35 wherein the quality of the oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

[c38] 38.The method of claim 35 wherein the third proportional value is a β 3 value corresponding to the third gate voltage, the β 3 value is equal to [{ Δ ln[|the third gate leakage current|/ (|the third gate voltage|-|a flatband voltage(V_{fb})|) ^{2}]} ÷ { Δ [1 ÷ (|the third gate voltage|-|the flatband voltage|)]}].

[c39] 39.The method of claim 38 further comprises a step for plotting a β -V_g curve of each β value respectively corresponding to the first gate voltage, the second gate voltage and the third gate voltage versus the first gate voltage, the second gate voltage and the third gate voltage, a reference β -V_g curve for the unstress-induced oxide layer is compared with the β -V_g curve to monitor the quality of the oxide layer.

[c40] 40.The method of claim 39 wherein the β -V_g curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

[c41] 41.The method of claim 40 wherein the β value within the first region is zero to represent each gate leakage current flowing through the first gate being less than a predetermined current value, the absolute value of the β value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each gate leakage current flowing through the first gate, the β value within the third region crosses the reference β -V_g curve to

represent a plurality of carriers being trapped by the oxide layer.

[c42] 42.The method of claim 41 wherein the predetermined current value is 1.0×10^{-11} A.

[c43] 43.The method of claim 32 further comprises a step for plotting a $\beta - V_g$ curve of each β value versus each gate voltage, a reference $\beta - V_g$ curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the $\beta - V_g$ curve to monitor the quality of the tunnel oxide layer.